

WHAT IS CLAIMED IS:

- 1 1. A method of manufacturing a semiconductor device, comprising:
 - 2 forming a gate oxide over a substrate and a gate electrode over the gate oxide;
 - 3 implanting impurities into the substrate using the gate electrode as an implant
 - 4 mask to form lightly-doped regions in the substrate;
 - 5 forming a first spacer adjacent the gate electrode;
 - 6 implanting impurities into the substrate and through a portion of the lightly-doped
 - 7 regions using the first spacer as an implant mask to form deep source/drain regions in the
 - 8 substrate;
 - 9 forming a second spacer adjacent the first spacer;
 - 10 implanting impurities into the substrate using the second spacer as an implant
 - 11 mask to form a graded source/drain region in the substrate; and
 - 12 removing the second spacer.
- 1 2. The method as recited in Claim 1, wherein said first spacer comprises a nitride.
- 1 3. The method as recited in Claim 1, wherein said second spacer comprises an oxide.
- 1 4. The method as recited in Claim 3, wherein the second spacer is a low-temperature
- 2 oxide having a thermal budget of less than 600C.
- 1 5. The method as recited in Claim 1, further including depositing a nitride layer over
- 2 the gate electrode and lightly-doped regions and forming the first spacer from the nitride
- 3 layer, and further including depositing an oxide layer over the gate electrode and lightly-
- 4 doped regions and forming the first spacer from the oxide layer.

1 6. The method as recited in Claim 1, further including forming a salicide over the
2 source/drain regions.

1 7. The method as recited in Claim 1, further including:
2 forming a dielectric over the gate electrode and the deep source/drain regions;
3 forming a contact opening through said dielectric; and
4 forming an interconnect in said contact opening, the interconnect being
5 electrically coupled to the deep source/drain regions.

1 8. A method of manufacturing a semiconductor device, comprising:
2 forming a gate oxide over a substrate and a gate electrode over the gate oxide;
3 implanting impurities into the substrate using the gate electrode as an implant
4 mask to form lightly-doped regions in the substrate;
5 forming a first spacer adjacent the gate electrode;
6 forming a second spacer adjacent the first spacer;
7 implanting impurities into the substrate using the second spacer as an implant
8 mask to form a graded source/drain region in the substrate;
9 removing the second spacer; and
10 implanting impurities into the substrate and through a portion of the lightly-doped
11 regions using the first spacer as an implant mask to form deep source/drain regions in the
12 substrate.

1 9. The method as recited in Claim 8, wherein said first spacer comprises a nitride.

1 10. The method as recited in Claim 8, wherein said second spacer comprises an oxide.

1 11. The method as recited in Claim 10, wherein the second spacer is a low-
2 temperature oxide having a thermal budget of less than 600C.

1 12. The method as recited in Claim 8, further including depositing a nitride layer over
2 the gate electrode and lightly-doped regions and forming the first spacer from the nitride
3 layer, and further including depositing an oxide layer over the gate electrode and lightly-
4 doped regions and forming the first spacer from the oxide layer.

1 13. The method as recited in Claim 8, further including forming a salicide over the
2 source/drain regions.

1 14. The method as recited in Claim 8 further including:
2 forming a dielectric over the gate electrode and the source/drain regions;
3 forming a contact opening through said dielectric; and
4 forming an interconnect in said contact opening, the interconnect being
5 electrically coupled to said source/drain regions.

1 15. A semiconductor device, comprising:
2 a gate structure formed over a semiconductor region;
3 a sidewall spacer formed along a sidewall of the gate structure;
4 a disposable spacer formed along an outer edge of the sidewall spacer;
5 a lightly-doped region formed in the semiconductor region to a first depth, the
6 lightly-doped region substantially aligned with the sidewall of the gate structure;
7 a deep source/drain region formed in the semiconductor region to a second depth
8 deeper than the first depth, the deep source/drain region substantially aligned with an
9 outer edge of the sidewall spacer; and
10 a graded source/drain region formed in the semiconductor region to a third depth

11 deeper than the second depth, the graded source/drain region substantially aligned with
12 an outer edge of the disposable spacer.

1 16. The device as recited in Claim 15, wherein the disposable spacer comprises a low-
2 temperature oxide having a thermal budget of less than 600C.

1 17. The device as recited in claim 15, wherein the lightly doped region, the deep
2 source/drain region, and the graded source/drain region are formed from impurities of the
3 same conductivity type.

1 18. The device as recited in claim 17, wherein the lightly doped region, the deep
2 source/drain region, and the graded source/drain region are formed from impurities of the
3 same material.

1 19. The device as recited in claim 15, further comprising a salicide region formed at
2 the surface of the semiconductor region adjacent the outer edge of the sidewall spacer.

1 20. The device as recited in Claim 15, wherein the semiconductor region comprises a
2 silicon-on-insulator substrate.